



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,357	02/06/2002	Michael D. Kilgore	M-11543 US	4288
34036	7590	03/29/2004	EXAMINER	
SILICON VALLEY PATENT GROUP LLP 2350 MISSION COLLEGE BOULEVARD SUITE 360 SANTA CLARA, CA 95054			GUERRERO, MARIA F	
		ART UNIT	PAPER NUMBER	
			2822	

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

10

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/072,357	KILGORE, MICHAEL D.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Maria Guerrero	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM  
 THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 15 December 2003.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-24 is/are pending in the application.  
 4a) Of the above claim(s) 21 and 22 is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-20,23 and 24 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

**DETAILED ACTION**

1. This Office Action is in response to the amendment filed December 15, 2003.

Claims 1-24 are pending.

***Election/Restrictions***

2. Newly submitted claims 21-22 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: the claims require the processing of a second wafer.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 21-22 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-11, 15-17, 19-20, and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwan et al. (U.S. 6,335,288) in view of Rice et al. (U.S. 5,925,212).

Art Unit: 2822

4. Kwan et al. teaches inserting a wafer into a reaction chamber, performing a plasma process on the wafer at a process temperature, cooling the wafer to a second temperature less than the process temperature, and removing the wafer from the reaction chamber (Fig. 1D, 3, col. 13, lines 47-67, col. 14, lines 5-10, 30-40, 50-55). Kwan et al. discloses the process temperature being greater than 400°C, the second temperature being less than 250°C or less than 150°C (col. 14, lines 23-40). In addition, Kwan et al. teaches the process being a plasma deposition of silicon dioxide for trench isolation and plasma deposition of fluorine doped silicon dioxide (Fig. 2, col. 1-10, col. 15, lines 5-25, col. 16, lines 35-36).

5. Kwan et al. does not specifically show the second temperature being the removal temperature and the specific temperature as claimed. However, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

6. Kwan et al. does not specifically show creating an idle condition plasma and cooling the wafer in the presence of the idle condition plasma. However, Kwan et al. teaches reducing the power supplied to a second level lower than the first level. In addition, Rice et al. discloses the step of creating an idle condition plasma and cooling the wafer in the presence of the idle condition plasma as conventional in the art (Fig. 4B, col. 23, lines 60-67, col. 24, lines 5-45).

Art Unit: 2822

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kwan et al. reference by specifying the use of the idle condition plasma as taught Rice et al. in order to avoid processing delays.

7. Claims 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwan et al. (U.S. 6,335,288) and Rice et al. (U.S. 5,925,212) as applied to claims- 11, 15-17, 19-20, and 23-24 above, and further in view of Chang et al. (U.S. 6,143,579).

Regarding claims 14 and 18, the combination of Kwan et al. and Rice et al. does not specifically show etching a photoresist and the wafer having a gate dielectric layer. However, Chang et al. teaches etching a photoresist and the wafer having a gate dielectric layer (col. 5, lines 28-30, 50-55).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Kwan et al. and Rice et al. by including the steps of etching the photoresist and forming the gate dielectric layer as taught Chang et al. because Kwan et al. suggested that other variations are included within the scope of this invention (Kwan et al., col. 15, lines 13-27).

8. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwan et al. (U.S. 6,335,288) in view of Wang et al. (U.S. 6,268,274).

Regarding claims 12-13, the combination of Kwan et al. and Rice et al. does not specifically show depositing a phosphorous-doped silicon dioxide layer. However, Wang et al. shows a plasma process to deposit a phosphorous-doped silicon dioxide layer (col. 6, lines 30-40).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Kwan et al. and Rice et al. by including phosphorous-doped silicon dioxide layer as taught Wang et al. because Kwan et al. suggested that different precursors can be used to form films of different composition (Kwan et al., col. 15, lines 15-25).

***Response to Arguments***

9. Applicant's arguments with respect to claims 1-20 and 23-24 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hander et al. (U.S. 6,403,501) (same Assignee) teaches a method of controlling deposition rate employing idle periods. .

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

Art Unit: 2822

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maria Guerrero whose telephone number is 571-272-1837.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Maria Guerrero  
Primary Examiner  
March 17, 2004